ANALOG DEVICES

AN-617
APPLICATION NOTE

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MicroCSP™ Wafer Level Chip Scale Package

by John Jackson and Alan O'Donnell

DESCRIPTION OF THE PACKAGE TECHNOLOGY

MicroCSP is a wafer level chip scale package, the only true chip size package. The die itself is the package. Eutectic solder bumps (63% tin, 37% lead) are connected to the active side of the die (either directly to the bond pads or through a redistribution layer). The MicroCSP part can then be mounted onto the customer's printed circuit board using standard surface-mount assembly techniques.

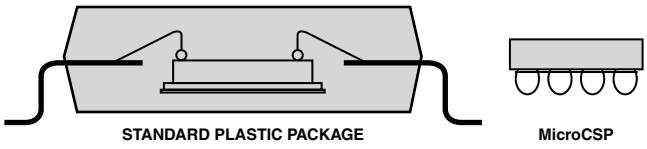

Figure 1. Standard Plastic Packaging vs. MicroCSP

MicroCSP technology offers a number of significant benefits in comparison to other packaging techniques, including the following:

- Improved electrical performance, e.g., reduced inductance due to the elimination of wire bonds and leads used in standard plastic packaging.
- Reduction in board space occupied as die size equals package size.
- Thinner package profile (with considerable weight reduction) due to the elimination of lead frame and molding compound.
- No underfill required, and standard SMT assembly equipment and processing can be used.
- High assembly yields can be realized from the self-aligning characteristic of the low mass die during solder attachment.

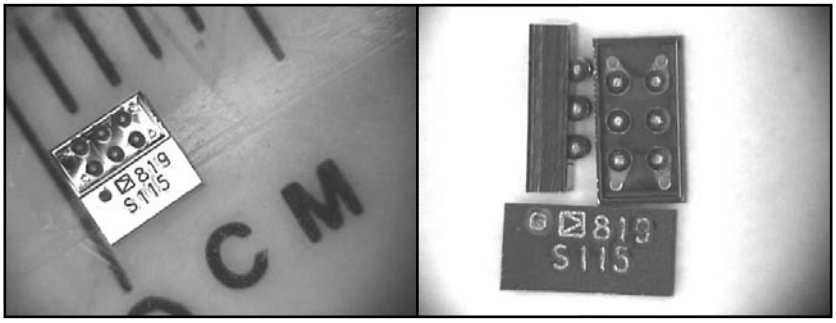

Figure 2. 3 3 2 Array (6 Input/Output) MicroCSP Parts

MicroCSP PACKAGE OPTIONS

All MicroCSP parts from ADI have a standard pitch of 0.5 mm and a standard bump diameter of either 0.320 mm (large bumps) or 0.180 mm (small bumps). For this reason, each array offered has a minimum die size (and thus package size) to accommodate the standard bumps and pitches.

A MicroCSP device occupies less board space than a standard plastic part with the identical number of I/Os. The diagram below shows a comparison between a standard 8-lead MicroCSP part and a list of standard plastic packages.

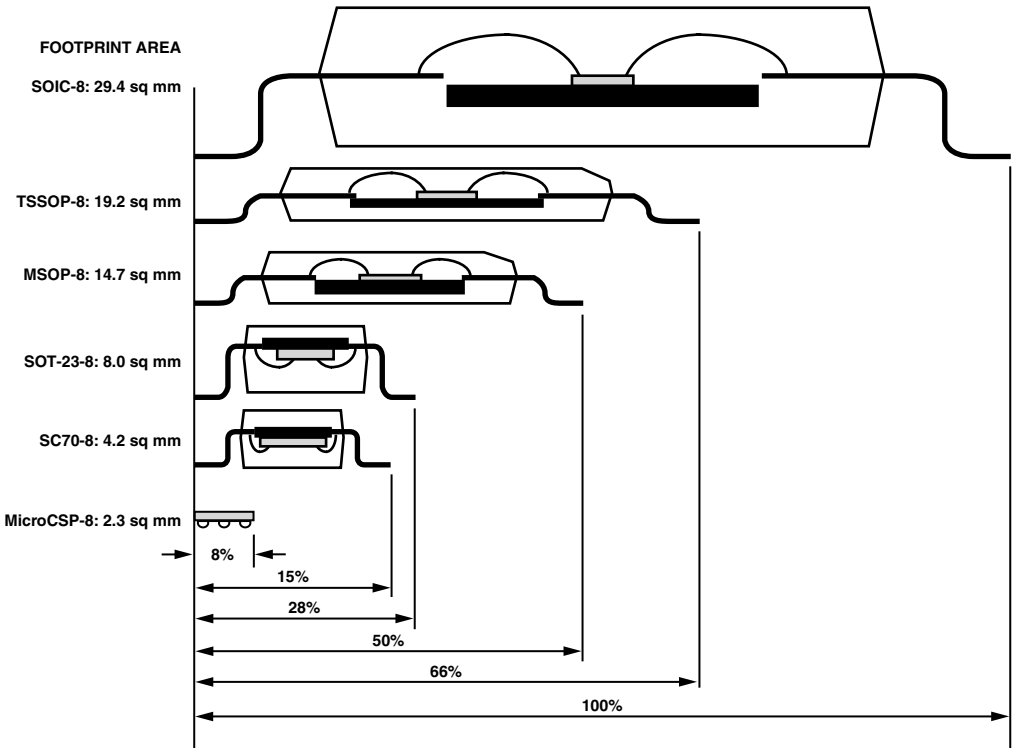

Figure 3. Board Area Comparison of Standard Plastic Packaging vs. MicroCSP

For an array pitch of 0.5 mm and a ball size of approximately 320 microns wide, the standard MicroCSP arrays offered include the following.

Table I. Minimum Die Size for Each MicroCSP Array

Array	Maximum I/O	Minimum Die Size
2 × 2	4	1.0 mm × 1.0 mm (39.4 mils × 39.4 mils)
2 × 1 × 2	5*	1.3 mm × 0.9 mm (51 mils × 36 mils)
2 × 3	6	1.0 mm × 1.5 mm (39.4 mils × 59.1 mils)
3 × 3	9	1.5 mm × 1.5 mm (51 mils × 59.1 mils)
3 × 4	12	1.5 mm × 2.0 mm (59 mils × 78.8 mils)
4 × 4	16	2.0 mm × 2.0 mm (79 mils × 78.8 mils)
4 × 5	20	2.0 mm × 2.5 mm (79 mils × 98.5 mils)
5 × 5	25	2.5 mm × 2.5 mm (99 mils × 98.5 mils)

* If the die is too small to accommodate 320 micron diameter balls, or a thinner mounted device is required, the smaller ball size (180 microns) can be considered. For example, a five ball 2 × 1 (center of die) × 2 array of 180 micron diameter balls will enable a die size of 1.3 mm × 0.9 mm to accommodate the five balls at 0.5 mm minimum spacing.

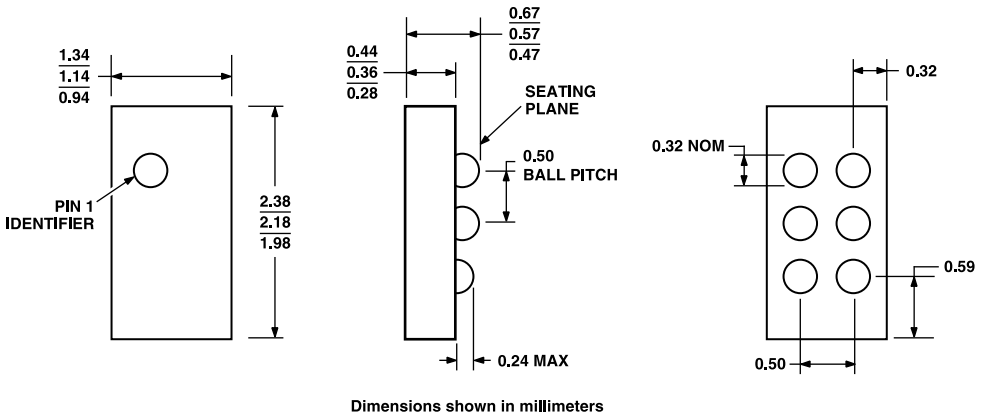

Figure 4. Typical Dimensions for a 3 × 2 MicroCSP Die (before Assembly)

BOARD/ASSEMBLY CONSIDERATIONS

The actual separation (standoff) after assembly will vary with the amount of solder screened on the substrate, weight of the die, wetted area, and so on. Typical dimensions for a die thinned to 14 mils are

Total Height: Large Ball –0.575 mm ± 0.03
Small Ball –0.460 mm ± 0.03

Standoff Height: Large Ball –0.22 mm ± 0.02
Small Ball –0.115 mm ± 0.05

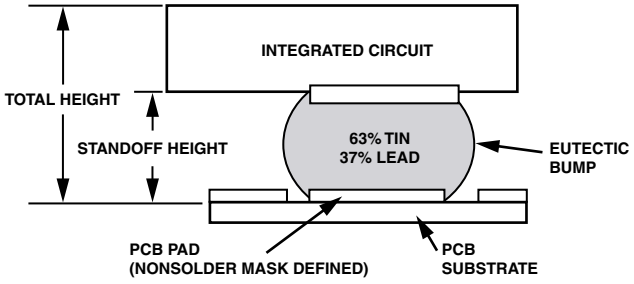

Figure 5. Typical MicroCSP Joint Cross Section after Reflow Attachment

For PCB fabrication, two different types of PCB pads/land patterns are used for surface-mount assembly:

1. Nonsolder Mask Defined (NSMD)—The metal pad on the PCB (to which a package I/O will be attached) is smaller than the solder mask opening.
2. Solder Mask Defined (SMD)—The solder mask opening is smaller than the metal pad.

The difference between these two land patterns is shown in Figure 6.

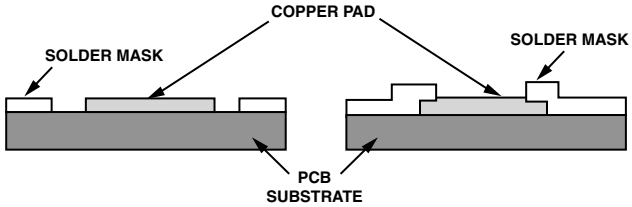

Figure 6. Cross Sections of NSMD and SMD Pads/Land Patterns

The solder mask opening defines the wettable area of the exposed copper conductor on the PCB. NSMD pads/land patterns provide a more robust solder joint than their SMD equivalents because the edge of the solder mask could be a stress initiator at the base of the solder ball. Also, for the NSMD configuration, the solder wets the sides of the copper pads, improving the strength of the solder joint between the MicroCSP part and the PCB. This can be seen through improved die shear and tensile pull strength values and thermal cycling reliability (compared to SMD). NSMD requires the solder-wetted area to be determined by the defined copper area, not by the solder mask. This is an advantage because the copper etch step is easier to control than the solder mask develop operation.

When designing the board, check the solder mask registration capability of the board manufacturer to ensure that the correct solder mask opening dimension is 50 µm either side of the copper pad. The actual size of the used copper pad should be between 80% and 100% of the diameter of the MicroCSP solder ball. It should be protected from oxidation by an organic surface protecting treatment. Copper thickness of less than 1 oz. is required to achieve the required definition.

Board Material

Standard epoxy glass substrates are compatible with MicroCSP. Assembly can be performed on standard epoxy glass substrate; however, changing from standard FR-4 to high temperature FR-4, which has a smaller thermal expansion, improves package reliability. However, the CTE of a PC board can also be affected by factors such as number of metal layers, laminate materials, trace density, operating environment, and site population density.

Board Thickness

Thinner boards are more flexible and consequently show greater reliability during thermal cycling. The standard board thickness used in the industry ranges from 0.4 mm to 2.3 mm.

Solder Paste Reflow and Cleaning

A solder paste with a maximum particle size of 40 µm or finer (no clean) paste is recommended. Because of potential corrosion issues, it is not advisable to use solder paste with active flux. Figure 7 shows a typical temperature/time profile for eutectic solder. A maximum reflow temperature of between 235°C to 240°C on the surface of the device is recommended with a nitrogen purge. Also, the oxygen content of the furnace must be monitored and kept below 100 ppm. Actual reflow temperatures need to be determined by the end user based on thermal loading effect measurements within the furnace.

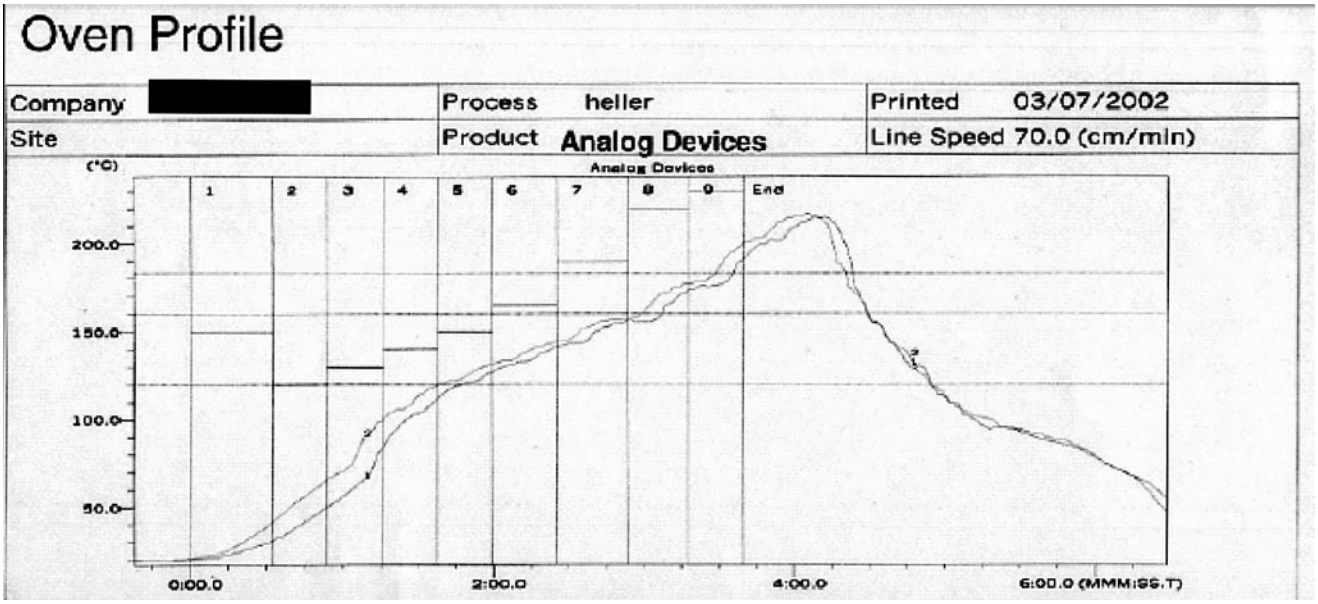

Figure 7. Typical Furnace Profile for Eutectic Solder

BOARD CONSTRUCTION CONSIDERATIONS

Due to the high pad density and the fine 0.5 mm pitch of the MicroCSP, any array larger than 3 × 3 bumps requiring connection to the inner bumps is unlikely to be routed on the top PCB layer only.

The traces (track and space) must fit between the limits of the solder mask openings. Routing on the top surface layer of the board, while possible, is usually not a feasible solution due to the limitations of the geometries imposed by the board fabrication technology. Typical PCB track and space rules are illustrated in Figure 8.

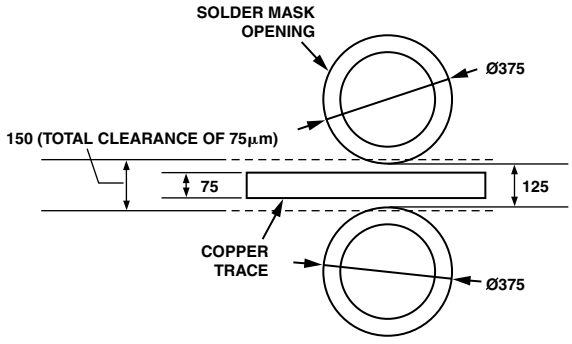

Figure 8. Typical PCB Track and Space Rules

As Figure 8 shows, for a pitch of 500 µm with a typical solder mask opening diameter of 375 µm, there is only 125 µm between the solder mask openings. Applying a typical track width and clearance of 75 µm each, this is greater than the required separation between the solder mask openings. Traces and separations of this size are not suitable for high yield manufacturing.

To achieve the necessary separation between pads and traces, using the dimensions outlined above, the pads need to be modified to nonstandard shapes to allow the traces to pass between them. An example of this is shown in Figure 9. However, because changing the PCB pad size and shape affects the actual joint between bump and PCB, this will also affect the reliability of the joint between the MicroCSP part and PCB and is not a recommended solution.

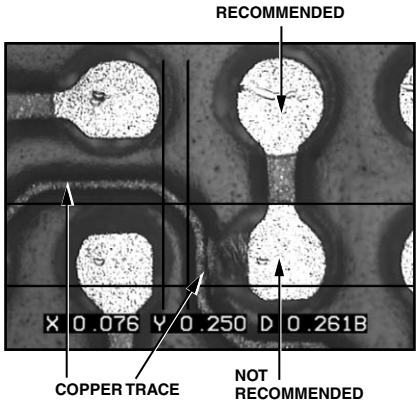

Figure 9. Undesirable Pad Geometries

MICROVIAS

An alternative to routing on the top surface is to route out on buried layers. To achieve this, the pads are connected to the lower layers using microvias. Standard vias are drilled approximately 300 µm with a pad of approximately 400 µm or more. Placing these standard vias is impossible, because an electrical short would result from insufficient clearance.

By placing the vias in the pad, the clearance is increased. However, a standard via opening of 300 µm would cause the solder to wick down into the via, causing weak or even open solder joints. Also, the capture pad is larger than the solder pad. The use of laser-drilled microvias will allow a hole of 100 µm to be drilled in the board, which, after plating, is further reduced to 50 µm. The resulting via hole diameter is reduced to the point where the solder will not wick down the via. Microvias are therefore a solution for routing to the inner rows of MicroCSP arrays.

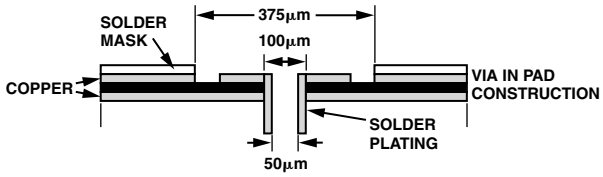

Figure 10. Typical Microvia Dimensions

FINE PITCH CONSIDERATIONS

Prior to screening solder on the PCB, check the pads for flatness and the presence of an organic surface protectant. For pads that use an electroplated nickel/immersion gold finish, a thickness of less than 0.5 microns is recommended. Also, the stencil should be laser-cut or electroformed and be 100 µm to 125 µm thick, with 250 micron square apertures with radius corners. For the fine pitch printing, a Type 3 no-clean paste is required and the usual in-process controls, e.g., print height, must be applied.

Automated placement with vision alignment should be used to place the parts and placement force should be kept to a minimum. Local fiducials are therefore required on the board. After reflow, sample testing is recommended of

- X-ray inspection for alignment, bridging, and voids
- Die shear and/or die pull

MicroCSP RELIABILITY

ADI follows a comprehensive new product/new process qualification procedure that is failure mechanism driven. Tests performed accelerate failure mechanisms that may occur under normal life conditions. Failure mechanisms associated with the MicroCSP process and appropriate stress tests are detailed in Table II.

Table II. MicroCSP Failure Mechanisms

Failure Mechanism	Description	Stress Test
Solder Fatigue	Results from the mismatch between the coefficient of the thermal expansion of the bumped chip and the substrate. This produces high stress at the solder joint and the bump fails at a low cycle fatigue.	Board Level Temperature Cycling
Corrosion	Corrosion of bump or UBM can result in several types of failures. Chemical reactions could result in open-circuit or dentritic formation can result in shorts or current leakage.	Autoclave HAST
Intermetalic Compound Formation	Can cause solder bump failure due to the excessive formation of intermetalics that can cause solder joint enbrittlement.	High Temperature Storage
Thermomigration/ Electromigration	Describes the migration of bump solder over time, excessive tin/copper, or tin/nickel could result in an open bump at the UBM/solder interface.	High Temperature Operating Life (HTOL)
Silicon Cratering	Is the fracture of the silicon under the bump during the bumping process or flip chip assembly resulting in open circuits. The primary reliability factors for controlling silicon cratering are the UBM material, UBM design/process, bump allowance, and manufacturing environment.	Bump/Die Shear

Table III. Reliability Qualification Results (3 × 2 Ball Array)

Stress Test	Conditions	Test Duration	Sample Size	Qty. Fail
Temperature Cycling	JEDEC-STD-22, Method A104 –40°C/+125°C, One cycle per hour.	1,000 Cycles	135	0
Autoclave	JEDEC-STD-22, Method A102 121°C/15 psi/100% rh	168 Hours	135	0
HAST	JEDEC-STD-22, Method A110 130°C/15 psi/85% rh	96 Hours	135	0
High Temperature Operating Bias	MIL-STD-883 Method 1005 125°C	1,000 Hours	132	0
High Temperature Storage	MIL-STD-883 Method 1008 150°C	1,000 Hours	135	0

For the purpose of reliability stress testing, the MicroCSP was mounted on a carrier PCB.

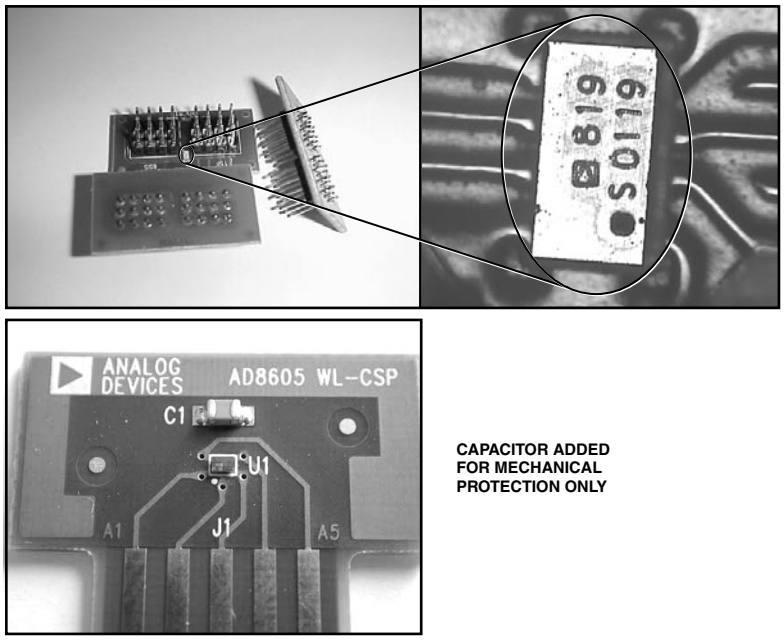

Figure 11. Examples of MicroCSP Reliability Test Boards

The usual package-related effects due to the encapsulant surrounding the die rarely impact an encapsulant-free MicroCSP package. For example, high temperature electrical failure is often due to movement of ionic impurities derived from the molding compound. Also, moisture can become trapped within the encapsulant and popcorning or corrosion may occur. Neither of these failure modes is observed with MicroCSP packaging technology. Nevertheless, because the die is mounted on a printed circuit board, second-level packaging concerns, such as solder fracture during thermal cycling, need to be considered.

SIMULATION OF SOLDER FATIGUE

As mentioned above, solder fatigue is affected by many variables, such as

- Board design—composition (number of copper layers), thickness, NSMD opening, composite expansion in all dimensions
- Pad size compared to the wetted area on die
- Solder composition and material properties, such as elastic modulus, plasticity, CTE, creep
- Temperature range and dwell at temperature extremes
- Ball size and distance from the center of the array to the furthermost ball (known as the distance from the neutral point—DNP)

ADI has performed stress modeling to understand both published and internally generated reliability predictions. It has also investigated the variables that can lead to failure. Specific solder ball arrays can be modeled to reinforce internally generated reliability data. Note that the maximum recommended die size for a MicroCSP is 3 mm × 3 mm. Beyond that, underfill is required to maintain solder joint integrity.

REWORK

MicroCSP rework is similar to that of a ball grid array. The board is baked to prevent moisture damage on rework, and the part for rework is heated to approximately 190°C. At this temperature, the solder is molten, and the device is removed with a vacuum wand or tweezers.

The pads need to be dressed, refluxed, and the replacement part precision placed at the site. Reflow is accomplished in a similar manner to removal, with a nozzle-directed hot air flow.

SHIPPING MEDIA

MicroCSP die are shipped in tape and reel. Pocket tape is dimensioned according to the size of the die, with an additional 0.13 mm added to the length, width, and depth. Static dissipative polymer is used for the tape fabrication. An example is shown in Figure 12.

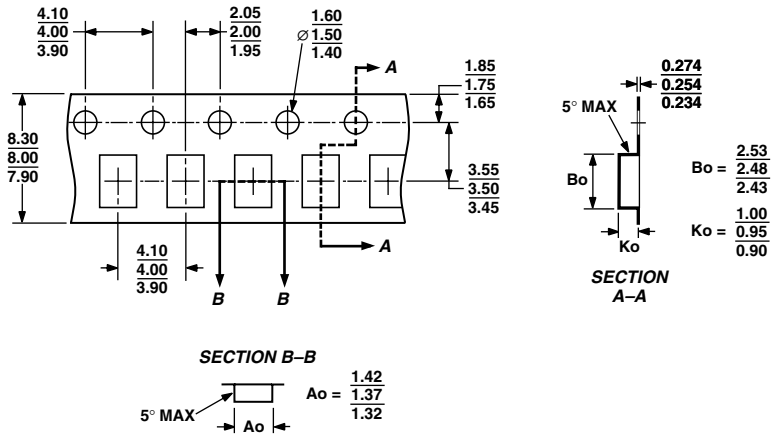

Figure 12. Typical Dimensions for MicroCSP Tape and Reel to Transport a Die 1140 µm × 2180 µm × 558 µm

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